SBS-IF Portable Design Conference

SMBus 2.0 in Systems with I²C*

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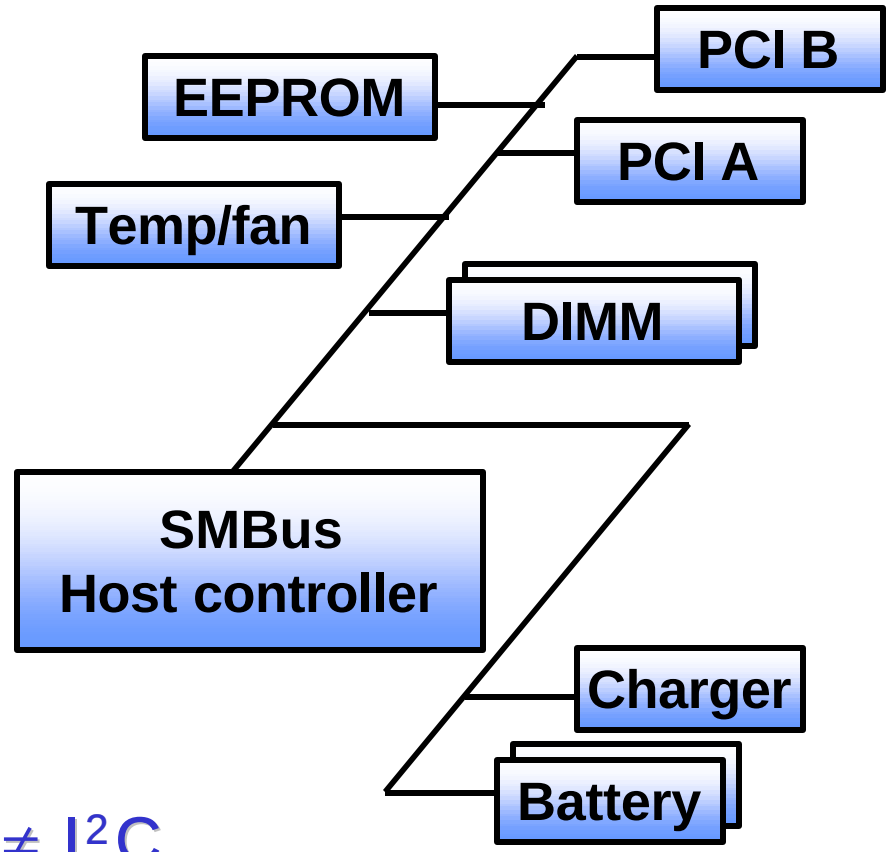
Collateral references

- S. Williams, D. Stolitzka and C. Laney, “SMBus 2.0 Released”, IDF August 2000
- T. Slaight, “SMBus and I²C Interoperability”, Intel Corp., Dec 2001
- SMBus Specification, ver. 2.0
  - SMBus website: http://www.smbus.org
- SMBus ECN to PCI 2.2 Specification
  - PCI SIG website: http://www.pcisig.com

System Management SMBus

Mixing SMBus and I²C devices, can I get in trouble?

- SMBus layers used throughout system
- Designers mix-in I²C due to availability
- DC electrical level incompatibilities and AC timeout issues will arise!



SMBus ≠ I²C

System Management SMBus

DC parameters matter

V_{DD} = 3.3V ± 10%

DC parameter comparison between SMBus devices						
Symbol	Parameter	Std I²C mode device		SMBus device		Units
		MIN	MAX	MIN	MAX	
V_{IL}	Fixed input level	-0.5	1.5	-	0.8	V
	V_{DD} related input level	-0.5	0.89V ~~$0.3V_{DD}$~~	N/A	N/A	V
V_{IH}	Fixed input level	3.0	V_{DD}max+ 0.5	2.1	5.5	V
	V_{DD} related input level	2.54V ~~$0.7V_{DD}$~~	V_{DD}max+ 0.5	N/A	N/A	V
V_{HYS}	V_{IH}-V_{IL}	N/A	N/A	N/A	N/A	V
V_{OL}	V_{OL} @ 3mA	0	0.4	N/A	N/A	V
	V_{OL} @ 6mA	N/A	N/A	N/A	N/A	
	V_{OL} @ 350uA	N/A	N/A	-	0.4	
I_{PULLUP}		N/A	N/A	100	350	uA
I_{LEAK}		-10	10	-5	5	uA

V_{OL} @ 4mA	(SMBus high power)	0.4	V
I_{LEAK}	(SMBus high power)	10	µA

System Management SMBus

AC timing and timeouts matter

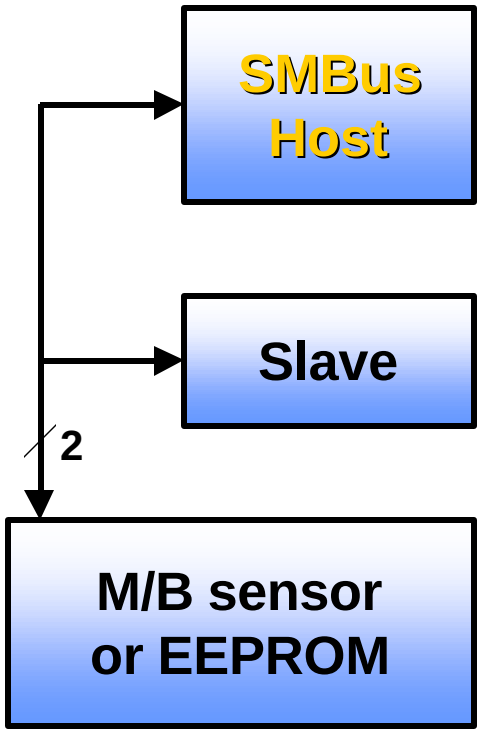
	I²C	SMBus
THD; DAT	0 ns	300 nS
RISE TIME	1000 ns from 0.89V to 2.54V	1000 ns from 0.65V to 2.25V
FALL TIME*	output stage: 250 ns from 2.54V to 0.89V	300 ns from 2.25V to 0.65V

- AC timing differences affect component selection
- SMBus uses bus timeouts; I²C has no timeouts and no minimum data rate

System Management SMBus

What if the bus is stuck?

- Host detects timeout
  - Watch for slave timeout
  - Send Stop condition
- Is the bus clear or at idle?
  - if SMBDAT (SDA) is low, the answer is **no**
  - A robust host will clock the bus until SMBDAT returns to high

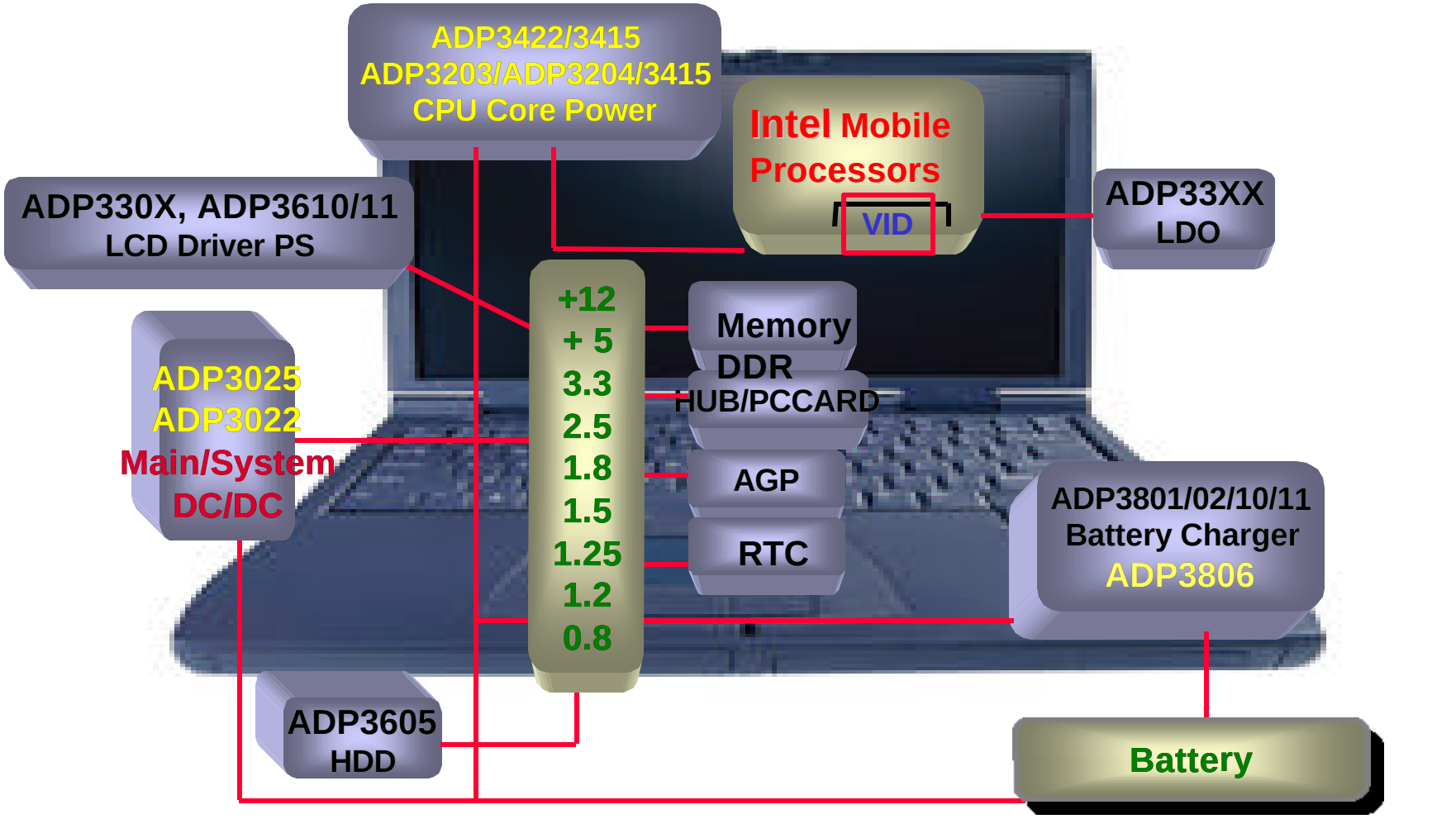


Designing for interoperability

- Host controllers could support dual protocol operation
  - Sink I_{OL} > 4mA
  - Output I^2C '1' and SMBus '0' levels.
  - Accept SMBus '1' and I^2C '0' levels.
  - Output data with SMBus hold time
  - Accept data with I^2C hold time
  - Watch for mid-byte start and stop conditions
  - Host monitors and proxies for device timeouts & clears the bus
  - Using the packet error checking will help robustness
- Mixing I^2C and SMBus masters can be problematic
  - I^2C Master-write timing can potentially cause problems with arbitration

System Management SMBus

Power IC's for portables



New ADP3806 battery charger

- Accurate to meet SBC spec
  - ±0.4% at 25°C
  - ±0.75% from 0°C to 85°C
- Fast
  - 500KHz switcher
  - small inductors
- Flexible
  - fixed output for 3 or 4 Li^+ cells
  - variable output versions
- Safe
  - Rail-to-rail current sensing